Features

- Single Supply Voltage, Range 3V to 3.6V
- 3-volt Only Read and Write Operation
- Software Protected Programming
- Fast Read Access Time – 120 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 40 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (128 Bytes/Sector)
  - Internal Address and Data Latches for 128 Bytes
- Two 8K Bytes Boot Blocks with Lockout
- Fast Sector Program Cycle Time – 20 ms
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

1-megabit (128K x 8) 3-volt Only Flash Memory

AT29LV010A

Not Recommended for New Designs. Use AT29BV010A.

1. Description

The AT29LV010A is a 3-volt only in-system Flash programmable and erasable read only memory (Flash). Its 1 megabit of memory is organized as 131,072 bytes by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 40 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

To allow for simple in-system reprogrammability, the AT29LV010A does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV010A is performed on a sector basis; 128 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

4.8 Optional Chip Erase Mode

The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4.9 Boot Block Programming Lockout

The AT29LV010A has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29LV010A blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

4.9.1 Boot Block Lockout Detection

A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location 1FFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

5. Absolute Maximum Ratings*

Temperature Under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. DC and AC Operating Range

		AT29LV010A-12	AT29LV010A-15	AT29LV010A-20	AT29LV010A-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply[1]		3.3V ±0.3V	3.3V ±0.3V	3.3V ±0.3V	3.3V ±0.3V

Notes: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

2 Not recommended for New Designs.

7. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A16 = V_{IL}, A9 = V_H,[3] A0 = V_{IL}	Manufacturer Code[4]
				A1 - A16 = V_{IL}, A9 = V_H,[3] A0 = V_{IH}	Device Code[4]
Software[5]				A0 = V_{IL}, A1 - A16 =V_{IL}	Manufacturer Code[4]
				A0 = V_{IH}, A1 - A16 =V_{IL}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code is 1F. The Device Code is 35.
5. See details under Software Product Identification Entry/Exit.

8. DC Characteristics

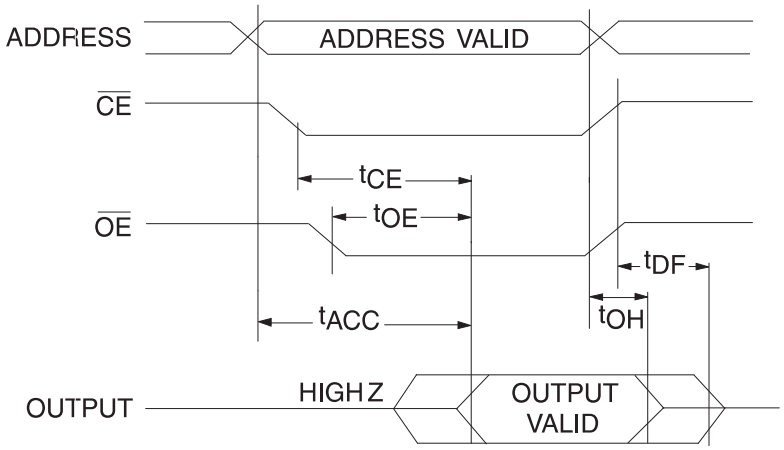
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		40	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

9. AC Read Characteristics

Symbol	Parameter	AT29LV010A-12		AT29LV010A-15		AT29LV010A-20		AT29LV010A-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	50	0	70	0	100	0	120	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	30	0	40	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

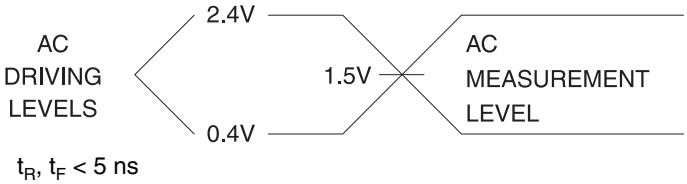
Note: Not recommended for New Designs.

10. AC Read Waveforms[1][2][3][4]



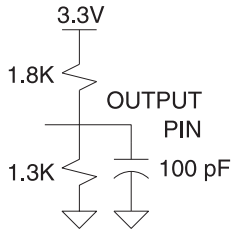
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

12. Output Test Load



13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

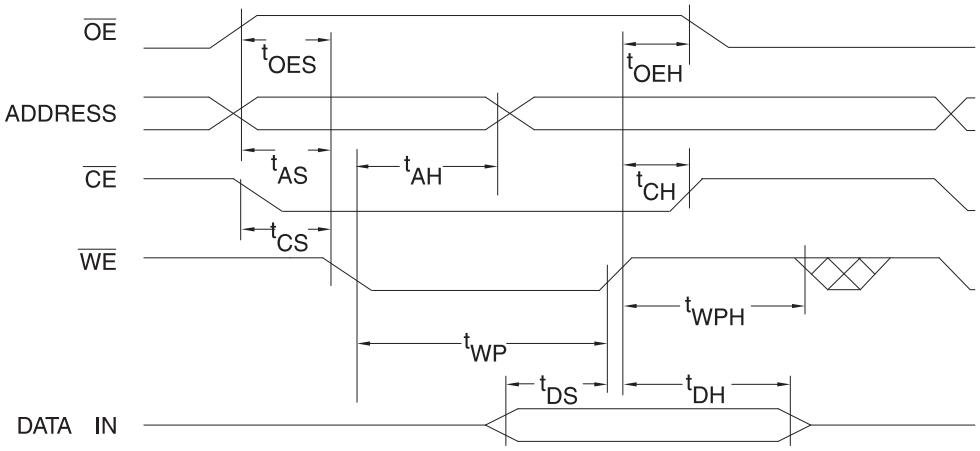
Note: 1. These parameters are characterized and not 100% tested.

14. AC Byte Load Characteristics

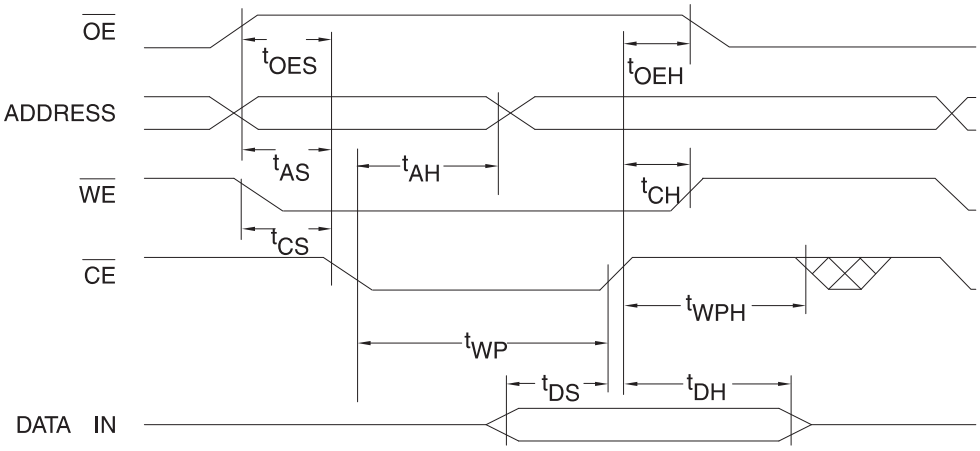
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

15. AC Byte Load Waveforms(1)(2)

15.1 $\overline{WE}$ Controlled



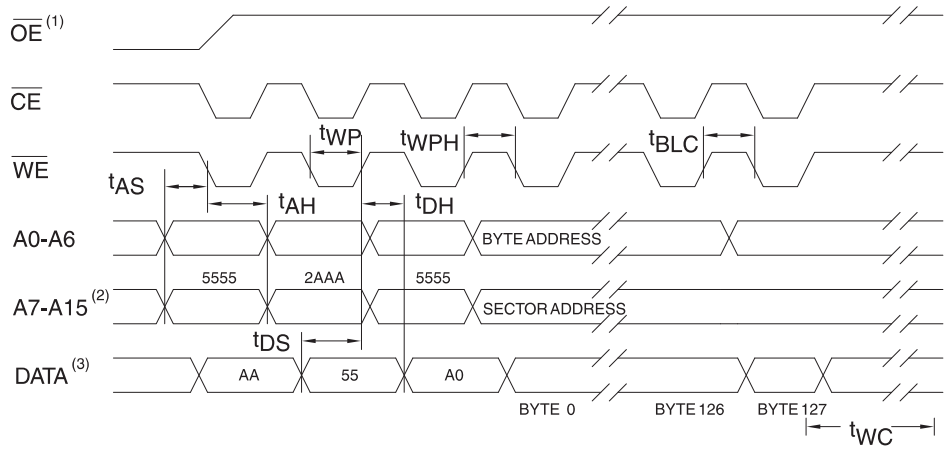
15.2 $\overline{CE}$ Controlled



16. Program Cycle Characteristics

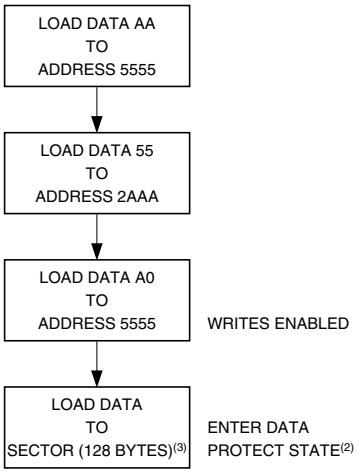
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

17. Software Protected Program Waveform



Notes:
1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. All bytes that are not loaded within the sector being programmed will be indeterminate.

18. Programming Algorithm(1)



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 128 bytes of data **MUST BE** loaded.

26. Ordering Information

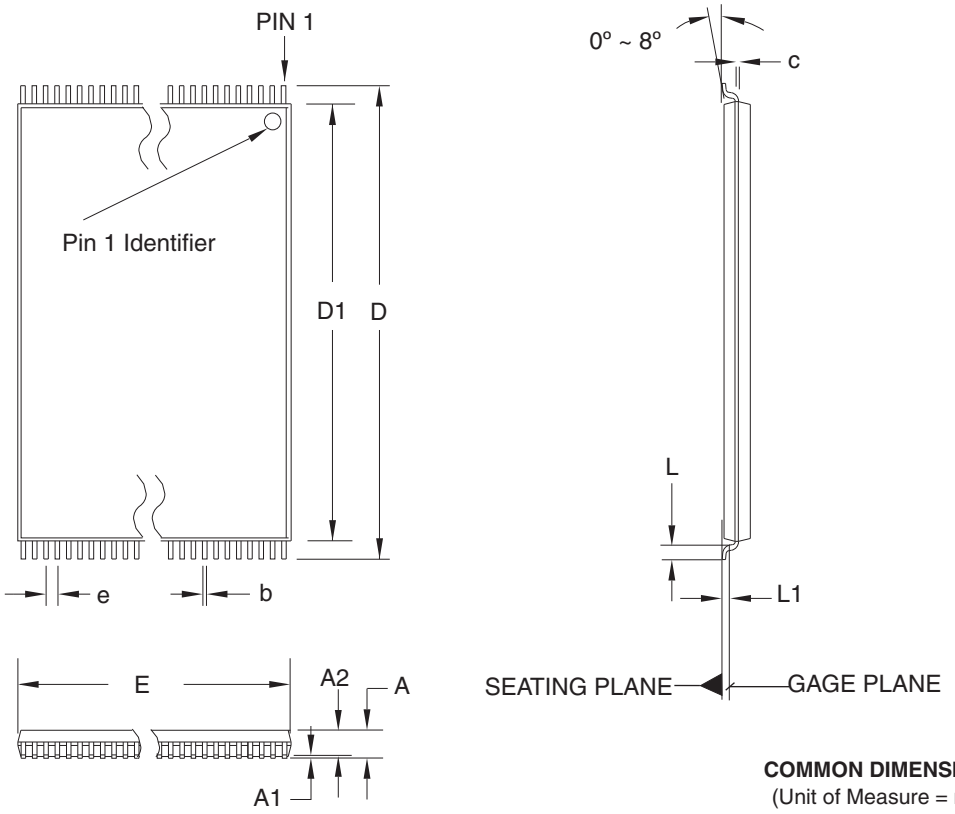
26.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	15	0.04	AT29LV010A-12JC AT29LV010A-12TC	32J 32T	Commercial (0° to 70° C)
	15	0.05	AT29LV010A-12JI AT29LV010A-12TI	32J 32T	Industrial (-40° to 85° C)
150	15	0.04	AT29LV010A-15JC AT29LV010A-15TC	32J 32T	Commercial (0° to 70° C)
	15	0.05	AT29LV010A-15JI AT29LV010A-15TI	32J 32T	Industrial (-40° to 85° C)
200	15	0.04	AT29LV010A-20JC AT29LV010A-20TC	32J 32T	Commercial (0° to 70° C)
	15	0.05	AT29LV010A-20JI AT29LV010A-20TI	32J 32T	Industrial (-40° to 85° C)
250	15	0.04	AT29LV010A-25JC AT29LV010A-25TC	32J 32T	Commercial (0° to 70° C)
	15	0.05	AT29LV010A-25JI AT29LV010A-25TI	32J 32T	Industrial (-40° to 85° C)

Note: Not recommended for New Designs.

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32-Lead, Thin Small Outline Package (TSOP)

27.2 32T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B