National Semiconductor

PRELIMINARY

ADC3511 3½-Digit Microprocessor Compatible A/D Converter
ADC3711 3¾-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

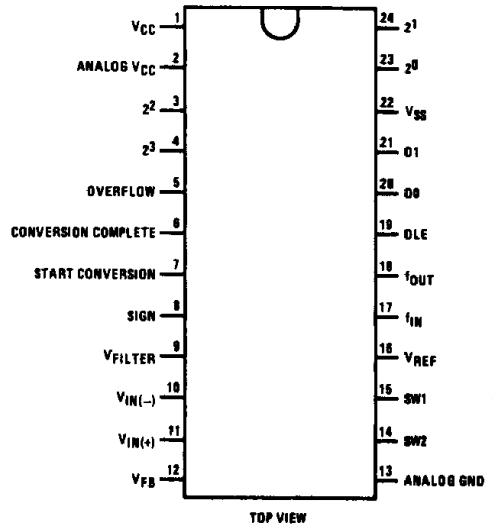
- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output
- ADC3511 equivalent to MM74C937
- ADC3711 equivalent to MM74C938-1

Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Dual-In-Line Package



Order Number ADC3511CCN or ADC3711CCN
NS Package N24A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at T_A = 25°C	500 mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD Susceptibility (Note 5)	TBD V

DC Electrical Characteristics ADC3511CC, ADC3711CC

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage (Except f_{IN})		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage (Except f_{IN})				1.5	V
$V_{IN(1)}$	Logical "1" Input Voltage (f_{IN})		V_{CC}−0.6			V
$V_{IN(0)}$	Logical "0" Input Voltage (f_{IN})				0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except 2^0, 2^1, 2^2, 2^3)	I_O = 360 μA	V_{CC}−0.4			V
$V_{OUT(1)}$	Logical "1" Output Voltage (2^0, 2^1, 2^2, 2^3)	I_O = 360 μA	V_{CC}−1.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (SC, DLE, D0, D1)	V_{IN} = V_{CC}		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (SC, DLE, D0, D1)	V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	All Outputs Open		0.5	5.0	mA

AC Electrical Characteristics ADC3511CC, ADC3711CC

V_{CC} = 5V; T_A = 25°C, C_L = 50 pF; t_r = t_f = 20 ns; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
f_{OSC}	Oscillator Frequency			0.6/RC		Hz
f_{IN}	Clock Frequency		100		640	kHz
f_{CONV}	Conversion Rate	ADC3511CC ADC3711CC		f_{IN}/64,512 f_{IN}/129,024		conversions/sec conversions/sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns
t_{pd0}, t_{pd1}	Propagation Delay D0, D1, to 2^0, 2^1, 2^2, 2^3	DLE = 0V		2.0	5.0	μs
t_{pd0}, t_{pd1}	Propagation Delay DLE to 2^0, 2^1, 2^2, 2^3			2.0	5.0	μs
t_{SET-UP}	Set-Up Time D0, D1, to DLE	t_{HOLD} = 0 ns		100	200	ns
t_{PWDLE}	Minimum Pulse Width Digit Latch Enable (Low)			100	200	ns

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Converter Characteristics

ADC3511CC, ADC3711CC $4.75 \le V_{CC} \le 5.25V$; $-40°C \le T_A \le +85°C$, $f_c = 5$ conv./sec (ADC3511CC); 2.5 conv./sec (ADC3711CC); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
	Non-Linearity	$V_{IN} = 0-2V$ Full Scale $V_{IN} = 0-200$ mV Full Scale	−0.05	±0.025	+0.05	% of Full-Scale (Note 3)
	Quantization Error		−1		+0	Counts
	Offset Error	$V_{IN} = 0V$	−0.5	+1.0	+3.0	mV (Note 4)
	Rollover Error		−0		+0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	$T_A = 25°C$	−5	±1	+5	nA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All typicals are given for $T_A = 25°C$.

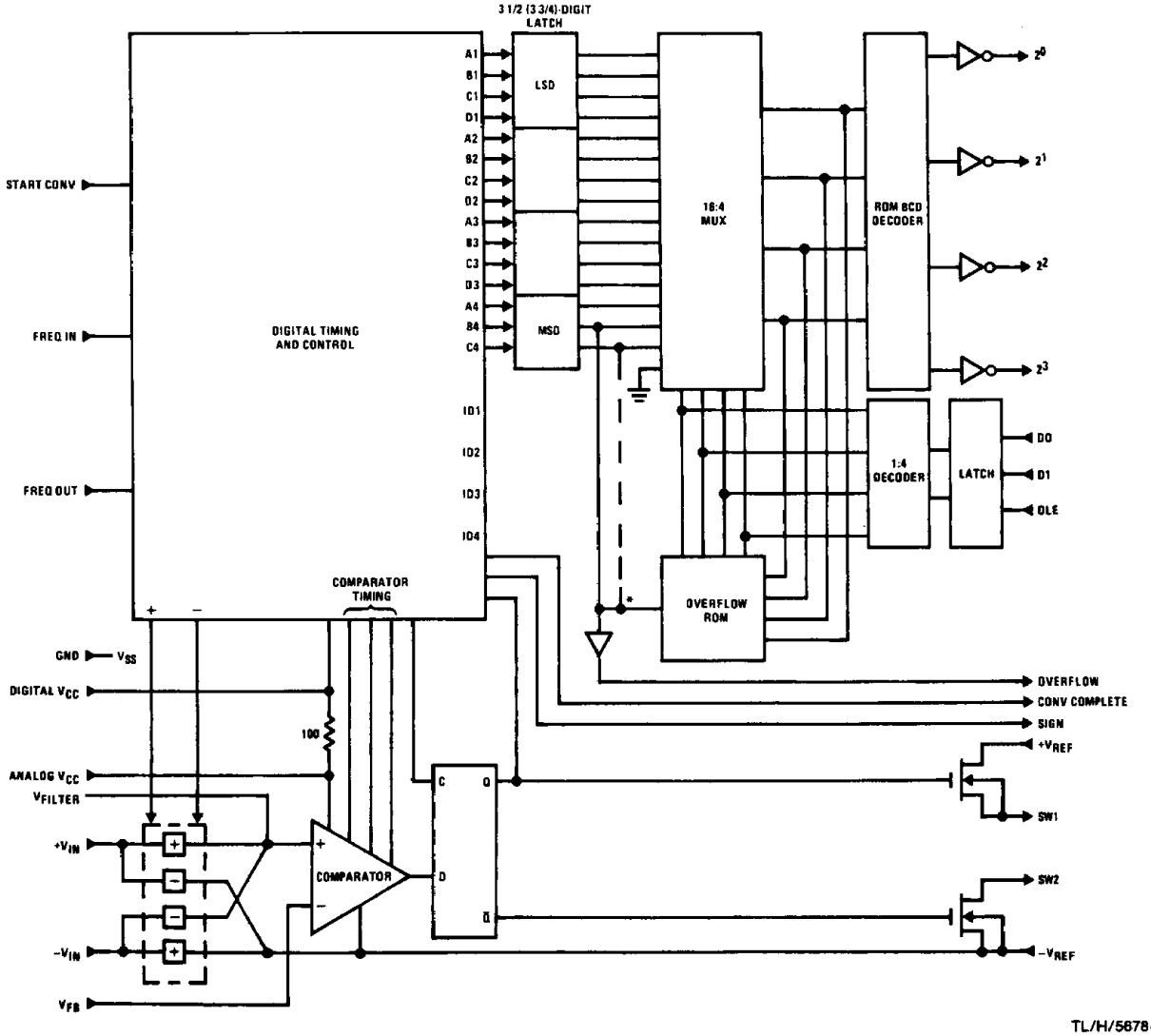
Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore 0.025% of full-scale = ½ count and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 count.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

Note 5: Human body model, 100 pF discharged through a 1.5Ω resistor.

Block Diagram

ADC3511 3 ½-Digit A/D (*ADC3711 3 ¾-Digit A/D)



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Applications Information

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure 1*. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT}=V_{REF}$ and if Q is at a low level $V_{OUT}=0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\frac{t_{ON}}{t_{ON}+t_{OFF}} = V_{REF}\,(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$V_{FB}=V_{REF}$ (duty cycle)

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$V_{IN}=V_{FB}=V_{REF}$ (duty cycle)

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$f=(\text{duty cycle})\times(f_{IN})$

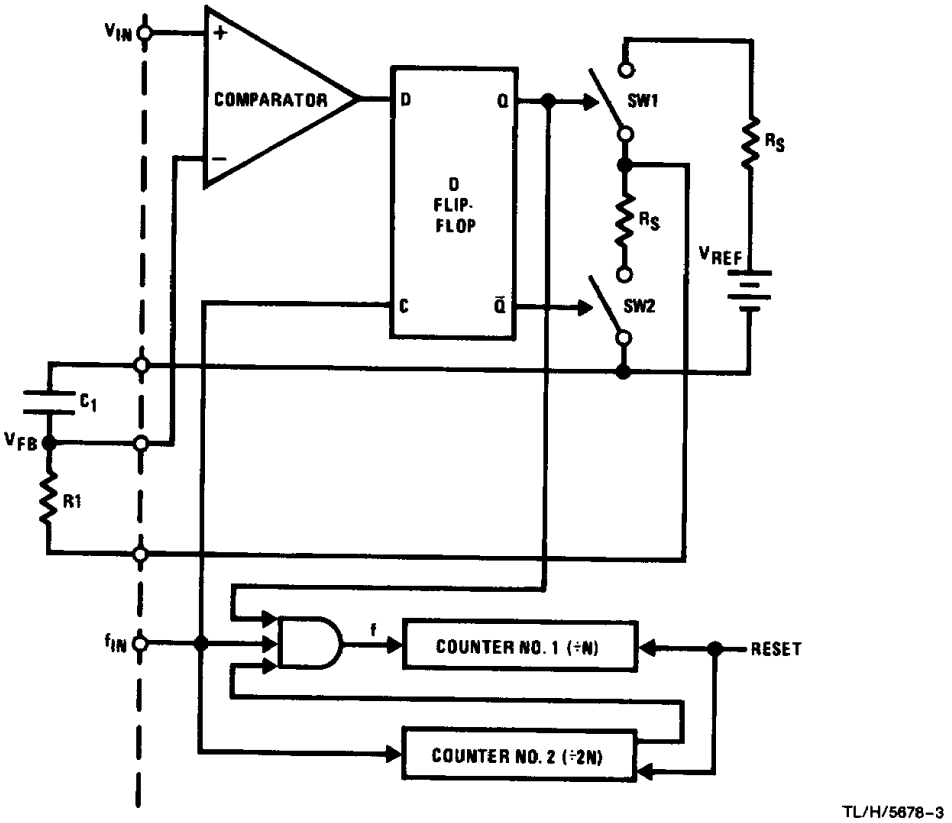
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(f_{IN})/N} = \frac{(\text{duty cycle})\times(f_{IN})}{(f_{IN})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N=2000.

For the ADC3711 N=4000.



$V_{IN}=V_{FB}=V_{REF}\times(\text{duty cycle})$

$f=(\text{duty cycle})\times f_{IN}$

$$\text{Count in counter no. 1} = \frac{f}{(f_{IN})/N} = \frac{(\text{duty cycle})\times f_{IN}}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

Applications Information (Continued)

GENERAL INFORMATION

The timing diagram, shown in *Figure 2,* gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the digit latches are updated at a rate equal to 64,512 × $1/f_{IN}$ for the ADC3511, or 129,024 for the ADC3711.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the digit latches. This information will remain in the digit latches until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to $64 \times 1/f_{IN}$ on the ADC3511, or $128 \times 1/f_{IN}$ on the ADC3711.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADC3511 and ADC3711 are always continuously converting the analog voltage present at their inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the digit latches.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3,* the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 × $1/f_{IN}$ (129,024 × $1/f_{IN}$ for the ADC3711) and the minimum time is 256 × $1/f_{IN}$ (512 × $1/f_{IN}$) for the ADC3711).

SYSTEM DESIGN CONSIDERATIONS

The ADC3511 and ADC3711 have reduced the problem of high resolution, high accuracy analog-to-digital conversion to nearly the level of simplicity, economy, and compactness usually associated with digital logic circuitry. However, they are truly high precision analog devices, and require the same kind of design considerations given to all analog circuits. While great care has been taken in the design of the ADC3511 and ADC3711 to make their application as easy as possible, in order to utilize them to their full performance potential, good grounding, power supply distribution, decoupling, and regulation techniques should be exercised.

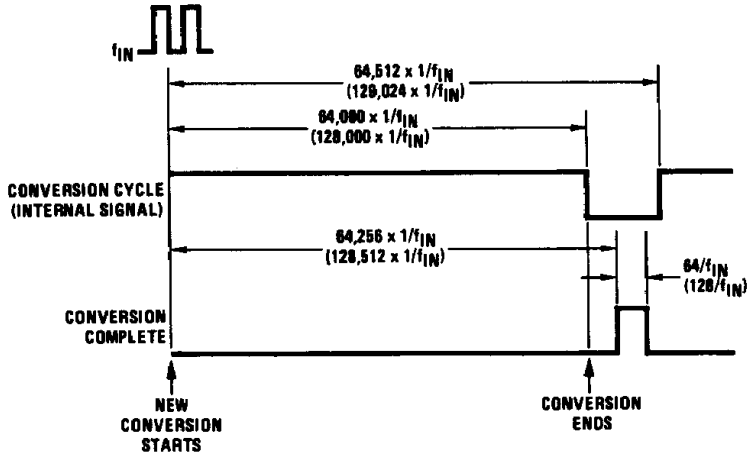


FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation (Times Shown in Parentheses are for the ADC3711)

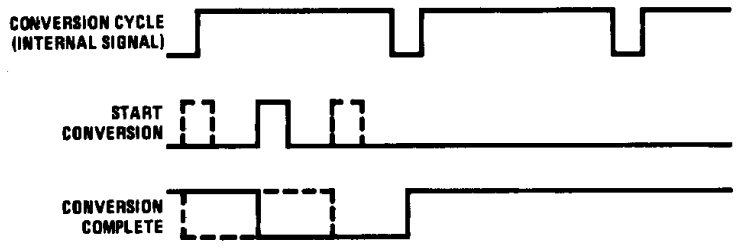


FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Truth Table

DIGIT SELECT INPUTS			SELECTED DIGIT
DLE	D1	D0	
L	L	L	Digit 0 (LSD)
L	L	H	Digit 1
L	H	L	Digit 2
L	H	H	Digit 3 (MSD)
H	X	X	Unchanged

L = low logic level

H = high logic level

X = irrelevant logic level

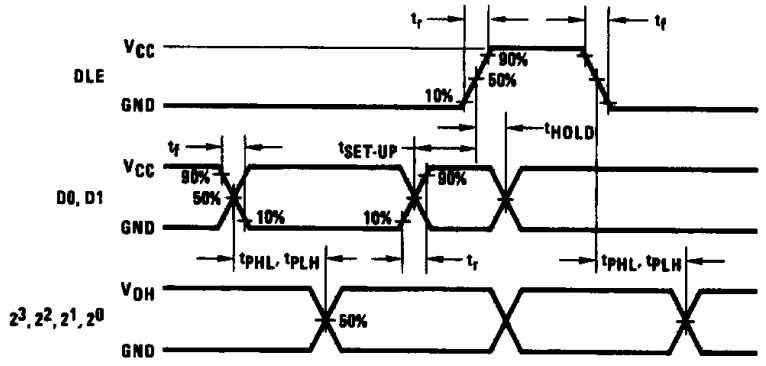
The value of the Selected Digit is presented at the 2^3, 2^2, 2^1 and 2^0 outputs in BCD format.

Note 1: If the value of a digit changes while it is selected, that change *will* be reflected at the outputs.

Note 2: An overflow condition will be indicated by a high level on the OVERFLOW output (pin 5) and E16 in all digits.

Note 3: The sign of the input voltage, when these devices are operated in the bipolar mode, is indicated by the SIGN output (pin 8). A high level indicates a positive voltage, a low level a negative.

Timing Diagrams



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Typical Applications

Figure 4 shows the ADC3511 and ADC3711 connected to convert 0 to +2.000 volts full scale operating from a non-isolated power supply. (Note that the ADC3511 converts 0 to +1999 counts full scale, while the ADC3711 converts 0 to +3999 counts full scale.) In this configuration the SIGN output (pin 8) should be ignored. Higher voltages can, of course, be converted by placing fixed dividers in the inputs, while lower voltages can be converted by placing fixed dividers in the feedback loop, as shown in *Figure 6.*

Figures 5 and *6* show systems operating with isolated supplies that will convert both polarities of inputs. 60 Hz common-mode noise can become a problem in these configurations, so shielded transformers have been shown in the figures. The necessity for, and the type of shielding needed depends on the performance requirements, and the actual applications.

The filter capacitors connected to V_{FB} (pin 12) and V_{FILTER} (pin 11) should be of a low leakage variety. In the examples shown every 1.0 nA of leakage will cause approximately 0.1 mV error ($1.0 \times 10^{-9} A \times 100\ k\Omega = 0.1$ mV). If the currents in both capacitors are exactly equal however, little error will result since the source impedances driving both capacitors are approximately matched.

Typical Applications (Continued)

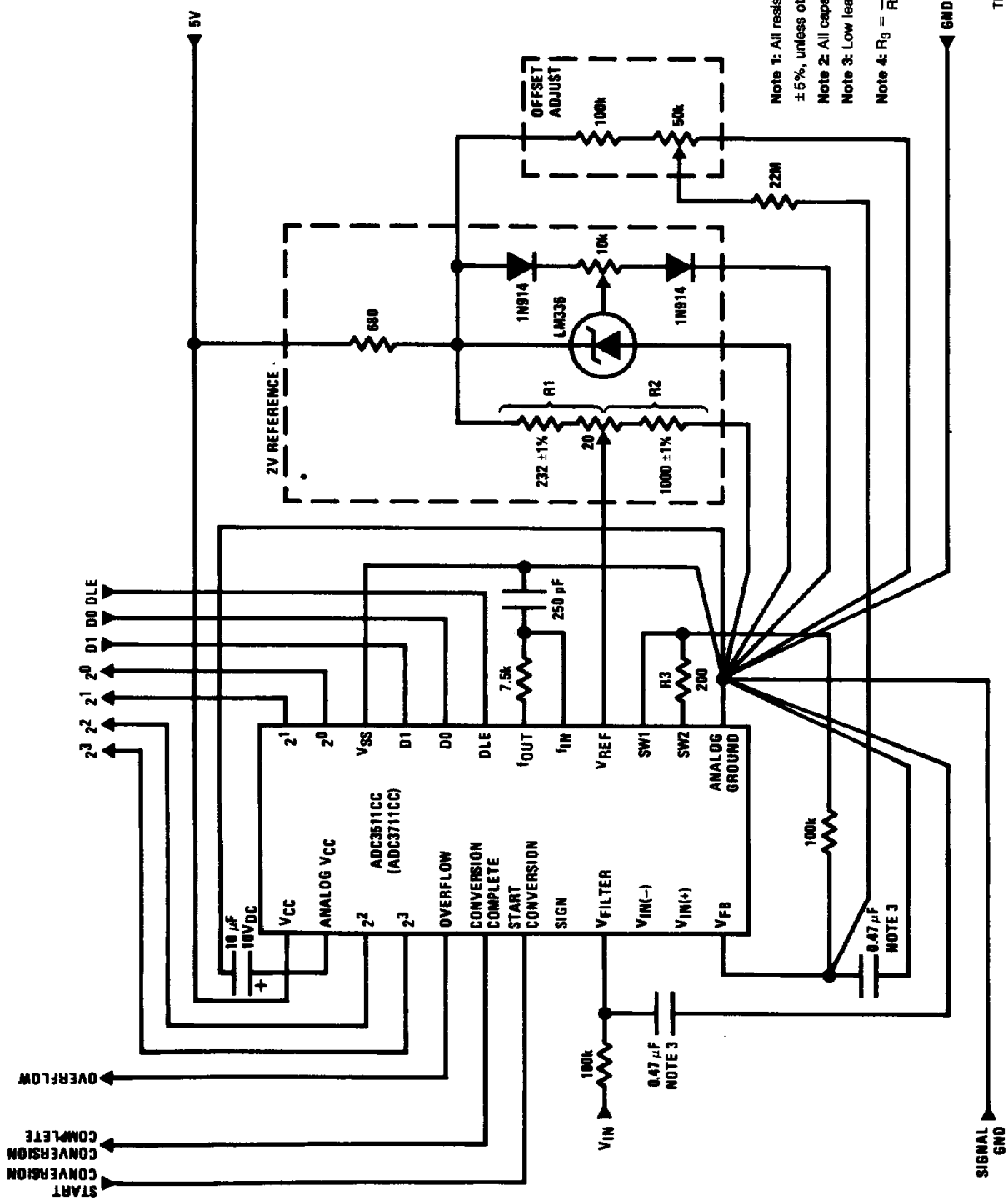

FIGURE 4. 3 ½-Digit A/D; +1999 Counts, +2.000 Volts Full Scale (3 ¾-Digit A/D; +3999 Counts, +2.000 Volts Full Scale)

Typical Applications (Continued)

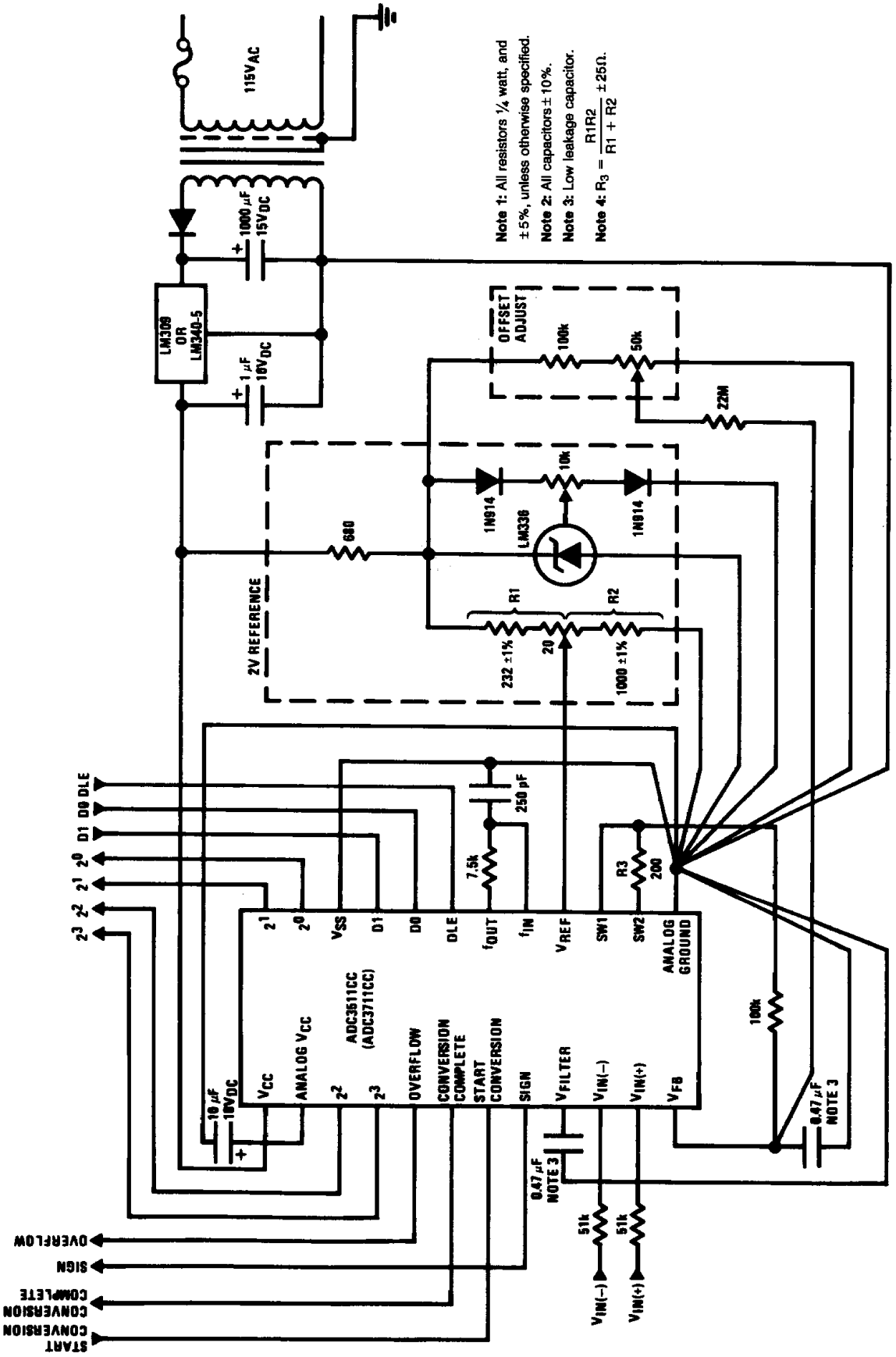

FIGURE 5. 3 ½-Digit A/D; ± 1999 Counts, ± 2.000 Volts Full Scale (3 ¾-Digit A/D; ± 3999 Counts, ± 2.000 Volts Full Scale)

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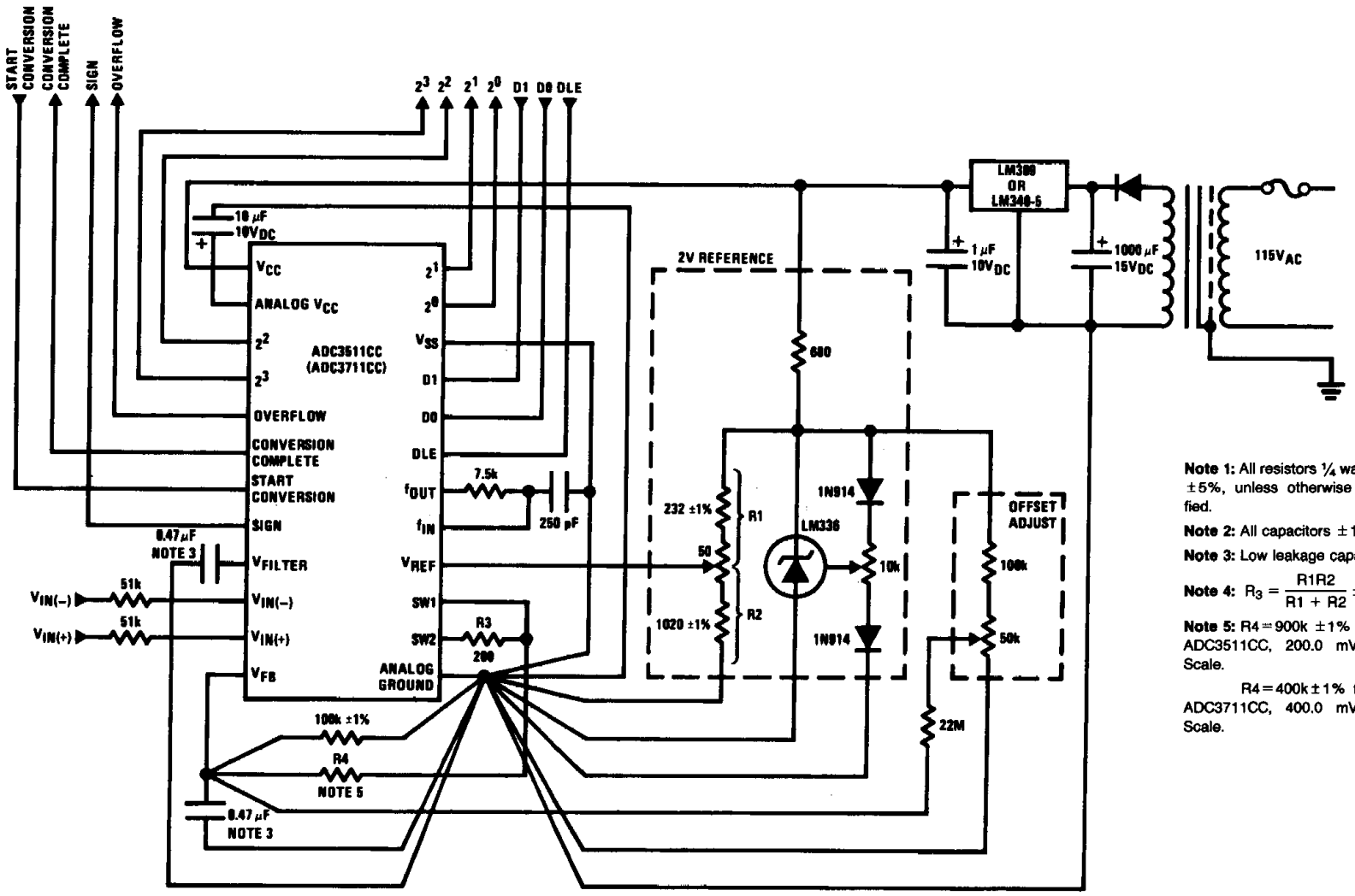
Typical Applications (Continued)



Note 1: All resistors ¼ watt, and ±5%, unless otherwise specified.

Note 2: All capacitors ±10%

Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 50\Omega$

Note 5: R4 = 900k ±1% for the ADC3511CC, 200.0 mV Full-Scale.

R4 = 400k ±1% for the ADC3711CC, 400.0 mV Full-Scale.

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FIGURE 6. 3 ½-Digit A/D; ±1999 Counts, ±200.0 mV Full Scale (3 ¾-Digit A/D; ±3999 Counts, ±400.0 mV Full-Scale)